Low Temperature Noise and Electrical Characterization of the Complementary Heterojunction Field-Effect Transistor (CHFET)

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Abstract—This paper discusses the electrical properties of the complementary heterojunction field-effect transistor (CHFET) at *4* K, including the gate leakage current, the subthreshold transconductance, and the input-referred noise voltage. The CHFET is a GaAs-based transistor analogous in structure and operation to silicon CMOS, and is being explored for possible application in readout electronics operating at *2-4* K. It is shown that CHFET is fully functional at *4* K, with no anomalous behavior, and that the drain current shows the expected dependence on device size and gate voltage. The input-referred noise is on the order of $1\ \mu V/\sqrt{Hz}$ at 100} Iz. The gate current is strongly dcpcndcnt on the doping at the gate edge, and is on the order of 10-14 amps for a 10x] O μm^2 device with the lightest doping. A simple multiplexed op-amp is presented, along with its transfer characteristics at 4 K.

1. INTRODUCTION

The availability of detector array readout electronics that can operate at and below 10 K would greatly simplify the design of low temperature focal planes for space telescope applications. Otherwise, the designer is forced to isolate the electronics in a warmer compartment and run a wire for each detector in the array from the focal plane cold head to the warmer electronics compartment. These wires arc susceptible to noise pickup and carry heat to the coldhead. In detector arrays used in space missions, the detected signals tend to be small, and there are severe constraints on the power or stored cryogen available for refrigeration, so the problems of noise pickup and heat conduction are particularly acute. Conversely, the availability of an analog amplifier and multiplexer that could be placed on the cold head in direct contact with the detector array could greatly increase the sensitivity and mission lifetime of space-based missions using detector arrays. For this reason, NASA has actively been exploring readout electronics functional below 10 K.

The major technical challenge involved in building very low temperature electronics is due to the phenomenon of carrier "freeze-out," in which carriers in a semiconductor lack the thermal energy to escape the donors and acceptors and are rc-trapped. This can result in the failure of any

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device made of that semiconductor. In addition, the trapping and de-trapping can occur randomly, causing the carrier concentration to fluctuate with time, which results in 1/f noise and operational anomalies such as kinks or hyst eresis. Alt bough silicon complementary metal-oxide-semiconductor (CMOS) technology is a logical choice for low power analog circuits, silicon is particularly susceptible to freeze-out, which makes it poorly suited for low temperature applications. Ordinary CMOS shows excessive noise, hysteresis, and kinks below 20 K. Development of CMOS optimized for operation below 10 K is underway [1], but has yet to demonstrate fully satisfactory results, especially for low power analog applications, By contrast, GaAs is far more resistant to freeze-out effects, making GaAs-based transistors an attractive alternative to silicon for low temperature applications. Several groups have begun to explore GaAs-based transistors for low temperature readout electronics applications [2-9]. For example, R. Kirschman ct. al., have studied commercial and foundry GaAs junction field-effect transistors (JFETs) and metal-Schottky field-effect transistors (MESFETs) at 4 K [2-4]. Camin, ct. al., have tested GaAs-based MESFETs for usc in particle detectors below 4 K [5]. Also, Kozlowski ct. al., have designed GaAs-based circuits for low temperature readouts [6].

JPL has been studying GaAs-based electronics for readout electronics applications in the 2-4 K temperature range. This has included an investigation of the low-temperature properties of a type of CMOS-like GaAs-based transistor called the complementary heterojunction field-eflcct transistor (CHFET). Although the CHFET was developed by 1 loneywell for high-speed, room-temperature digital applications [10], it has several features that indicate that it might be suitable for very-low temperature operation. The properties of the CHFET including the current-vohagc characteristics, gate leakage current, and noise voltage have been examined at 4 K, and are presented in the following sections.

II. THE STRUCTURE OF THE CHFET

A cross-section of the CHFET is shown in Fig. 1. Starting on a semi-insulating GaAs substrate, molecular beam cpitaxy (MBE) is used to grow a GaAs buffer layer, an InGaAs channel, a high aluminum mole-fraction AlGaAs dielectric layer, and a thin passivating GaAs cap layer. As grown, all of the layers arc undoped, except for the channel, which is deha-doped to make the turn on voltages of the n-channel and p-channel devices more symmetric. A well implant can be made at this point: p-type for n-channel devices and n-type for p-channel devices. The WSi gate is then deposited. An implant is then made to dope the region near the gate edge, using the gate to make it se]f-aligned. Sidewall spacers are then deposited on the gate edge, and the sow-cc and drain implants are done, sc]f-aligned to the sidewall spacers. This two-step implant allows the doping concentration in the sidewall region adjacent to the gate edge to be controlled independently of the source and drain doping concentration. The device is completed by adding ohmic contacts for the source and drain, and by doing an insulating isolation implant between devices.

The CHFET operates in enhancement mode in a manner completely analogous to that of silicon CMOS, with the AlGaAs layer playing the role of the oxide. A gate voltage draws electrons or holes into the channel where they are confined vertically by the AlGaAs dielectric. The carriers move laterally, and arc collected by the drain, The gate voltage modulates the channel charge density above threshold, and the channel potential below threshold.

The features of the CHFET that make it attractive for low temperature applications arc that it is a GaAs-based design, and so is less susceptible to freeze-out, and that it provides complementary transistors that simplify the design of low power circuitry. This is important, since any heat dissipation is an extra load on the refrigeration, so the power dissipation requirement is highly constrained. 1 lowever, there arc two areas of concern that must be addressed to determinc whether the CHFET will be suitable for low temperature readout applications. The first is the gate leakage current, which is expected to be considerably larger than that in CMOS because the potential barrier formed by the AlGaAs is much smaller than that for Si02. The second area of concern is the noise, which limits the sensitivity of detection.

in principle the CHFET structure can be fabricated such that every part is undoped except the source and drain which are degenerately doped. This makes it completely immune to freeze-out, and also makes the channel free of scattering centers, which should result in low noise at low temperatures. The devices which have been tested to date, however, were fabricated as part of larger lots which were optimized for high-speed, room-temperature, digital applications. Because the devices were not optimized in any way for low temperature operation, the noise at low temperatures may be artificially high. Nevertheless, this study has provided an indication of the feasibilit y of the Cl HFET for low temperature analog applications.

Two lots of CHFETs were fabricated. Each lot consisted of a series of chips, each containing a number of different sized n-channel and p-channel devices. The different chips explored process variations including the thickness of the AlGaAs dielectric, the presence or absence of a well implant and the presence of a buffer fabricated by low temperature MBE growth, with different thicknesses of spacers bet wccn the buffer and the channel. The devices in the second lot also included the use of gate sidewall spacers, and various spacer thicknesses and sidewall doping concentrations were explored.

111. THE CURRENT-VOLTAGE CHARACTERISTICS OF THE CHFET

The transistor curves at 4 K for a typical n-channel and a p-channel device are shown in Fig. 2. The data was measured using a HP4145B semiconductor parameter analyzer. The CHFET operates normally at 4 K without any anomalies, and the devices exhibit the expected dependence on gate voltage and device size. The subthreshold drain current vs. gate voltage is shown in Fig. 3. As expected, the current in the subthreshold region varies exponentially with gate voltage.

$$I_d = I_0 \exp(V_{gs}/V_a) \quad (1)$$

where I_d is the drain current, V_{gs} is the gate-source voltage, and V_a is a constant which we will refer to as the exponent voltage. The constant Va depends on the temperature and on the ratio of the change in channel potential to the change in gate-source voltage. Since the only doping in devices without a well implant is the small channel delta doping, the channel potential should follow the gate-source voltage in nearly a 1:1 ratio. This would imply that

$$Va = nkT/q \quad (2)$$

where T is the absolute temperature, and n is a constant close to 1. The exponent voltage Va vs. '1' is plotted in Fig. 4 for a 10x 10 μm^2 device without a well implant between 4 K and 260 K. Near room temperature V_a is a small factor larger than kT/q, while at low temperatures it deviates from this. The reason for the deviation is not known, At 4 K, V_a is approximately 17 times kT/q, which gives a corresponding sub-threshold normalized transconductance of 0.17 mS/mm for this 10x 10 μm^2 CHFET at 4 K and 10 nA drain bias current.

IV. THE GATE LEAKAGE CURRENT

The gate current of the first lot of CHFETs was examined in previous studies and has been shown to be duc to a combination of field-emission, thermionic-field-emission, thermionic-emission, and ohmic conduction, each of which is dominant for different values of the temperature and gate voltage [11, 12]. Below 10 K, the current for both positive and negative gate voltages is dominated by field emission. For reverse gate voltages (negative for n-channel CHFETs), the current is described well by the Fowler-Nordheim equation, while for forward gate voltages it is not. Devices of different gate lengths and widths were examined to determine whether the current was uniform over the gate area, or was concentrated at the gate edges. Any size dependence, however, was overwhelmed by a large device-to-device variation, The gate current-gate voltage curves tended to cluster when plotted on a semilog scale, and at any given voltage the current of about 80°/0 of the devices was within an order of magnitude. About 20°/0 of the device were outliers, with much higher currents, sometimes over five orders of magnitude more. It was concluded that the current might be dominated by tunneling through asperities at the gate edges, making the current level process dependent and somewhat random.

Measurements on the second lot of devices with the gate sidewall spacer provided new information [13, 14]. The data was measured with the source and drain grounded using an HP4145B semiconductor parameter analyzer, and is plotted for several typical devices in Fig. 5. The flat region at approximately 10-12 amps exhibited by some of the curves is due to the resolution limit of the 1+1)414511.

The gate current is strongly dcpcndcnt on both the sidewall spacer width and on the sidewall region doping level. The three solid curves represent devices with moderate sidewall doping and for spacer widths of 1000, 2000, and 3000 Å. The current decreases monotonically with increasing spacer width. "l'he dotted lines represent devices with a 3000 Å spacer, and with light, moderate, and heavy doping in the sidewall region, Again, the current increases strongly and

monotonically with increasing doping concent ration, The sample with the 1000 Å spacer and the sample with the heavy side wall region doping exhibit reverse gate current that is orders of magnitude larger that the other devices. In addition, the spread of the current is larger for these sets of devices, with many more outliers, so that the set of devices with heavy sidewall region doping and the set with the thin sidewall spacer do not exhibit any systematic size dependence, similar to the behavior of the first lot of devices, which did not include sidewall spacers.

The current for the devices with the widest sidewall spacer and light sidewall region doping, on the other hand, shows a regular size dependence. Both the forward and reverse currents scale linearly with width. This is shown in Fig. 6 which plots the current at –1 O V and +1.5 for 1 μm-long devices as a function of width. The reverse current does not show any systematic length dependence, while the forward current increases sub-linearly with increasing length. Since the channel is depleted for reverse voltages, the reverse current is expected to be dominated by tunneling at the gate edge, and should be independent of the length. For forward voltages, there is a sheet of inversion charge which can tunnel out over the entire area of the device, so it is possible that this current might scale linearly with the area. The fact that the actual dependence is sub-linear suggests that while this current is present, there is a component due to tunneling at the gate edge as well,

The drain current and the forward gate current for the device with the widest sidewall spacer and the light sidewall region doping are compared in Fig. 7. The data represented by the solid lines were recorded with the HP4145B parameter analyzer, and is accurate to 10-12 amps. A Keithley 617 electrometer was used in the integrating mode to measure the gate current down to about 10-14 amps, and this data is plotted in Fig. 7 as discrete circles. It can be seen from the subthreshold drain current data that it requires a gate voltage about 0.85 V to bias the device at about 10 nA, which is a reasonable value of bias current to use in low-power readout circuit applications. At this gate voltage the gate leakage current is on the order of 10-14 amps.

V. THE NOISE VOLTAGE

The input-referred noise voltage was measured using a feedback circuit that directly provided the input-referred noise voltage. The noise voltage for three different size n-channel CHFETs is shown in Fig. 8. The voltage noise of the largest device without the well implant is approximately $1\mu V/\sqrt{Hz}$ at 100 Hz. The noise decreases with increasing device size, an effect that has been observed in most t ypcs of transistors. The noise voltage for 50x50 μm^2 CHFETs with and without a well implant is shown in Fig. 9. The noise is increased by about an order of magnitude by the addition of the well implant. This is expected, since additional dopants tend to increase the trapping and scattering of carriers. The noise was also measured as a function of the temperature, drain bias current, and source-drain voltage. None of these had a very significant effect. The concentration of the channel delta-doping, the sidewall region doping, and the sidewall spacer thickness, likewise, did not have a significant effect on the noise.

VI. P-CHANNEL CHFETS

The p-channel CHFETs operate in an similar manner as the n-channel devices, but almost always with reduced performance. The gate leakage current is slightly higher for the p-channel devices, and the transconductance is slightly less, but the devices were in these respects quite comparable. On the other hand, the noise in the p-channel devices was several orders of magnitude higher. This is in contrast to silicon CMOS, in which p-channel devices normally have significantly lower noise than n-channel transistors. The discrepancy in the noise could be caused by the fact that the electron effective mass in GaAs is much smaller that for holes. This could imply that the holes in the p-doped channel arc freezing out.

VII. CHFET MULTIPLEXERS

Several different simple 8x1 multiplexer circuits were also fabricated and tested at 4 K. In each of these a voltage could be stored on eight capacitors that simulated a small linear array of detectors. Addressable readout electronics were connected to each capacitor and to common output circuitry which included a source follower output driver.

When tested, most of these circuits did not operate properly at 4 K. The p-channel devices used in these circuits appeared to be very leaky and even when they were turned off completely there was still significant conduction between the gate, source, and drain. This behavior is not understood, since the discrete p-channel CHFETs made from the same chips did not exhibit excessive leakage current. Since p-channel CHFETS were used in most of the circuits both to enable the capacitor reset and to enable the individual cells, it was consequently impossible to isolate the capacitor from the reset voltage and reset enable signal, or to de-select individual cells, which meant that these circuits did not function as multiplexer.

One circuit, however, used n-channel CHFETs to do the cell select, and it function as a multiplexer, although with limited performance. This circuit is called the switched op-amp multiplexer. Each cell consists of a n-channel differential pair, the sources of which are connected to an addressable n-channel CHFET current source. The drain of the inverting transistor from each pair is connected to a common p-channel active load. The output voltage is taken from this node and buffered through an n-channel source follower connected to an n-channel CHFET current source load. The cell is selected by sending a bias voltage to the addressable n-channel CHFET. Although the failure of the p-channel C} HFETs still made it impossible to turn off the capacitor reset voltage completely, and probably reduced the impedance of the inverter load, it was possible to see both inverting and non-inverting action in the device. A circuit schematic for the switched op-amp multiplexer is shown in Fig. 10. The inverting transfer characteristics for each cell measured at 4 K arc shown in Fig. 11. The voltage gain at 4 K is approximately 250.

VIII. SUMMARY

The CHFET has been shown to be completely functional at 4 K, with no anomalies or hysteresis. It has a clean subthreshold current-voltage characteristic and allows the capability of complementary devices. The gate leakage is strongly dependent on the doping concentration in the region adjacent to the gate, and a CHFET using a sidewall spacer and light sidewall region doping had a gate leakage current of approximately 10-14 amps for gate voltages that biased the device in the subthreshold region, The noise voltage is on the order of 1 $\mu V/\sqrt{Hz}$ at 1001 Iz for large n-channel CHFETs and 100 $\mu V/\sqrt{Hz}$ for p-channel CHFETs. It increases as the device size is reduced, or with the addition of a well implant. A multiplexed op-amp using CHFETs was designed, and was functional at 4 K.

The capability of complementary logic and anomaly-free performance at 4 K make the CHFET attractive for low-power, low temperature circuitry. While the existing (unoptimized) devices may be adequate for some applications, further technology development is desirable to reduce the gate leakage and noise, making the devices more widely applicable,

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FIGURES

Fig. 1: A cross-section of the complementary heterojunction field effect transistor (CHFET).

Fig. 2: The transistor curves for an n-channel and p-channel CHFET.

Fig. 3: The subthreshold current for various size n-channel CHFETs. The current was measured with an **11P414** 5B semiconductor parameter analyzer which has a sensitivity of approximately 10-12 amps.

Fig. 4: The exponential voltage V_a (from the sub-threshold current relation $I = I_0 \exp(V_{GS}/V_a)$) as a function of temperature plotted as circles for a 10X] O μm^2 n-channel CHFET. For comparison, the relation $V = kT/q$ is plotted as a solid line.

Fig. 5: The gate current vs. gate voltage for devices with different gate sidewall widths and different doping concentrations in the sidewall region adjacent to the gate.

Fig 6: The dependence of the gate current at $V_{GS} = -10$ V and + 1.3 V vs. width for 1 pm-long n-channel CHFETs with a 3000 Å gate sidewall space and light sidewall region doping.

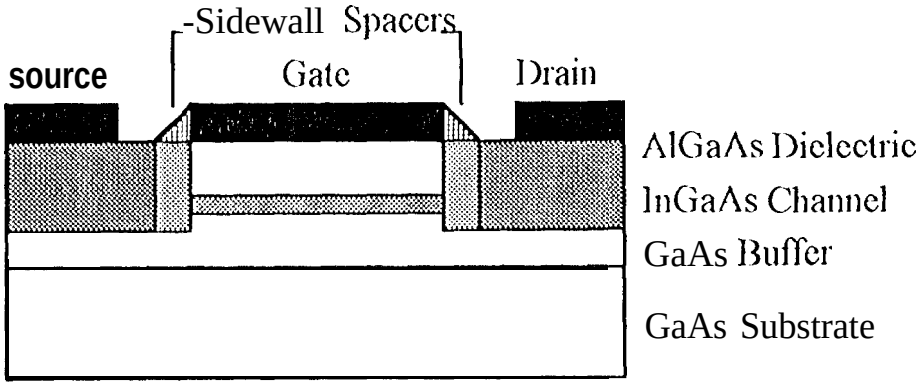
Fig. 7: Comparison of the drain current and the gate current in a CHFET with a lightly doped sidewall region and no well implant. The solid lines were measured with an HP4145B semiconductor parameter analyzer, which has a sensitivity of approximately 10-12 amps. The circles arc points taken with a Keithley 617 electrometer in the integrating (coulomb) mode.

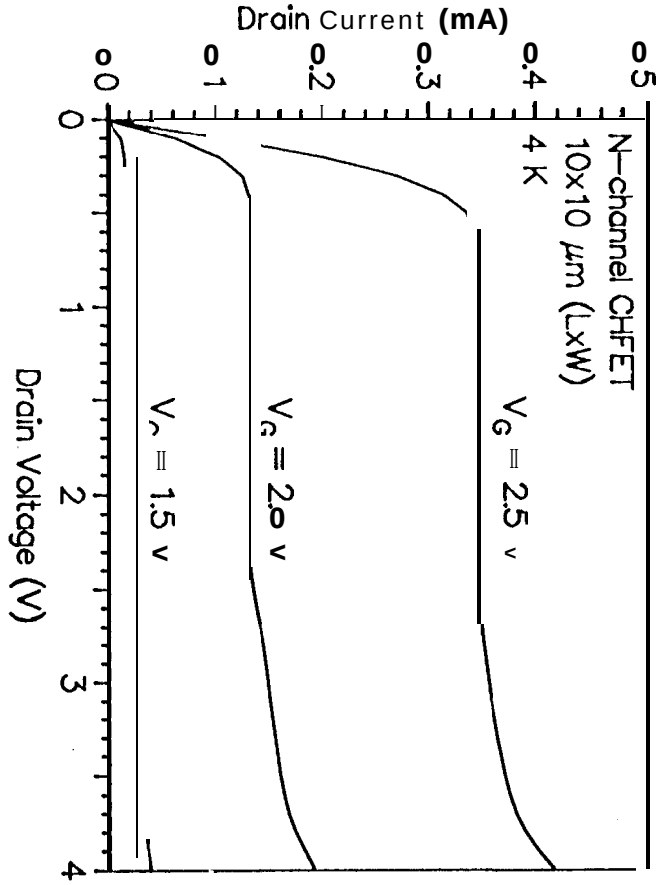
Fig. 8: A comparison of the input-referred noise voltage for different size CHFETs. For some reason, some of the devices showed a peak in the **noise at approximately** 501 Hz. Some sort of pickup is suspected, but its origin has not yet been found and is still under investigation,

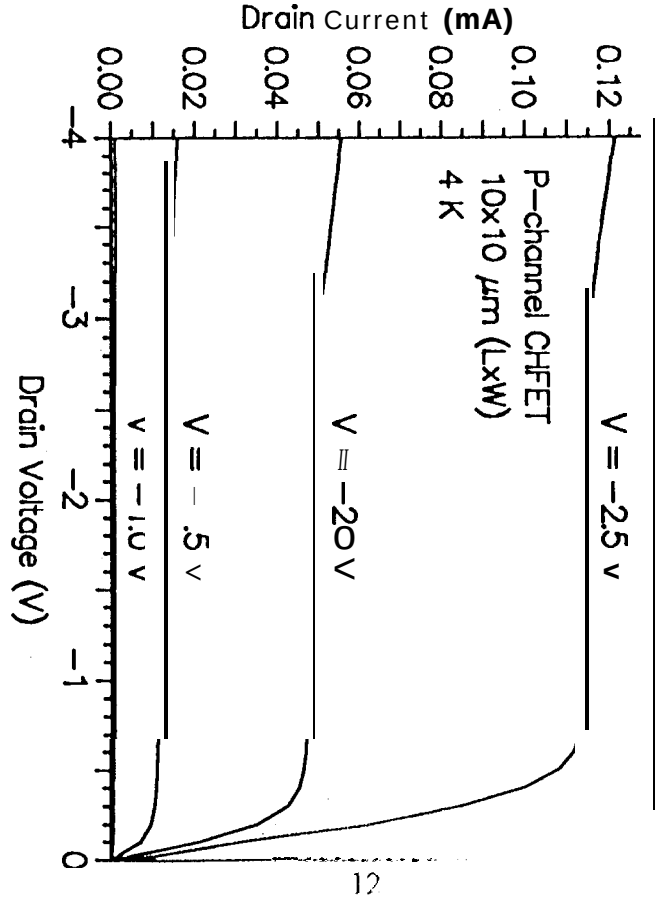
Fig 9. A comparison of the input-referred noise voltage for 50x50 μm^2 n-channel CHFETs with and without a well implant.

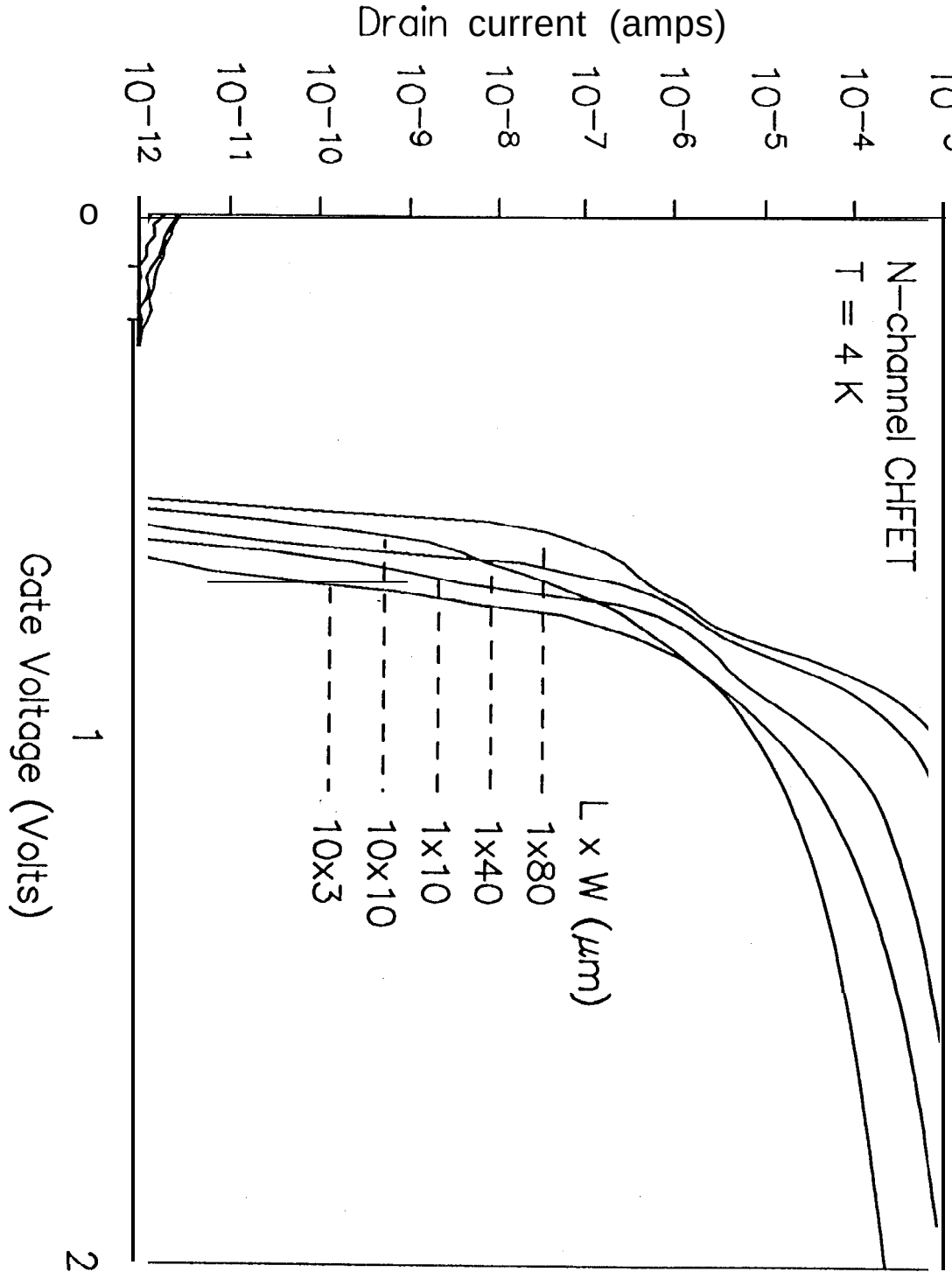
Fig. 10: The circuit schematic for a CHFET 8x1 switched op-amp multiplexer

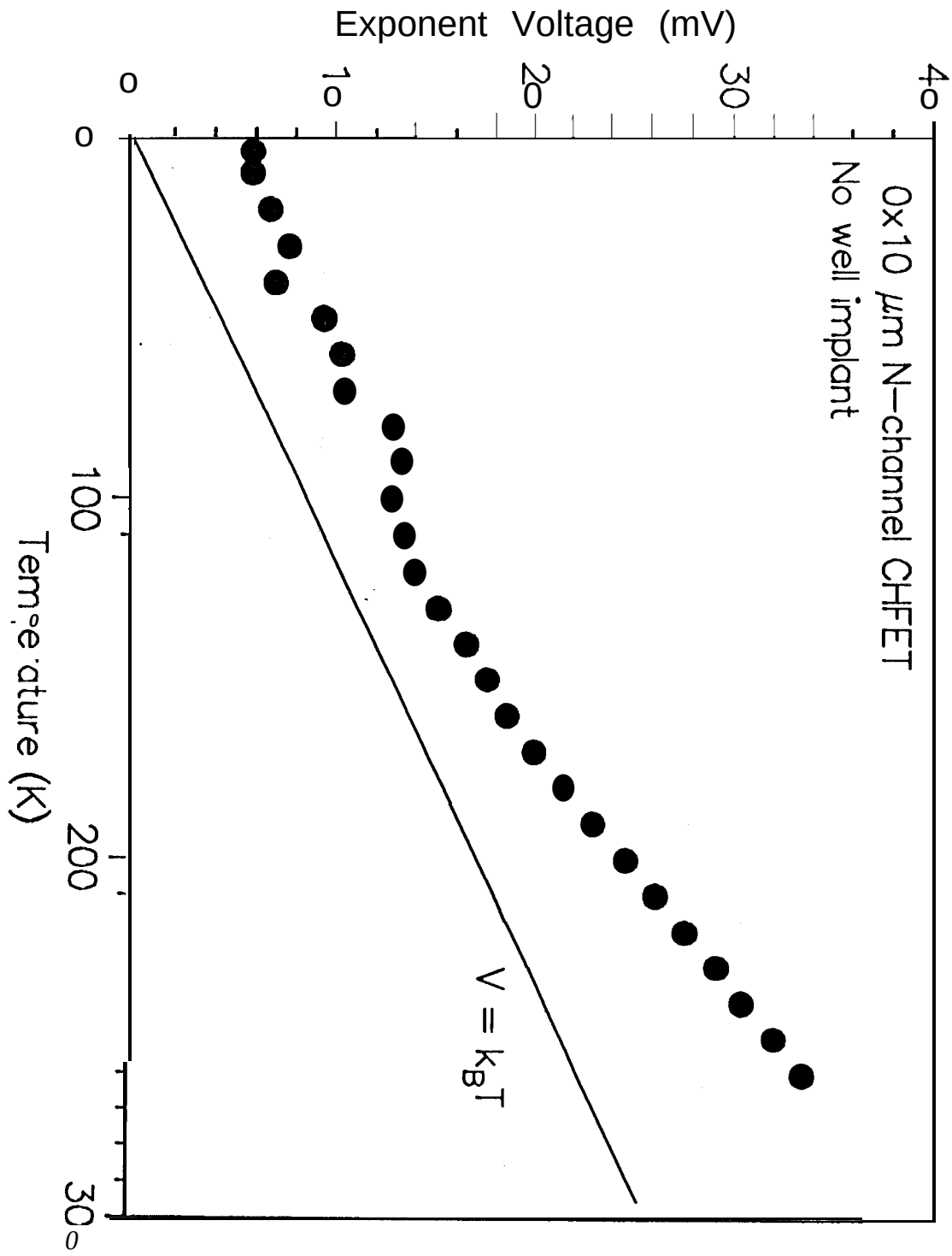
Fig. 11: The inverting transfer characteristics at 4 K for each cell of the 8x 1 switched op-amp multiplexer.

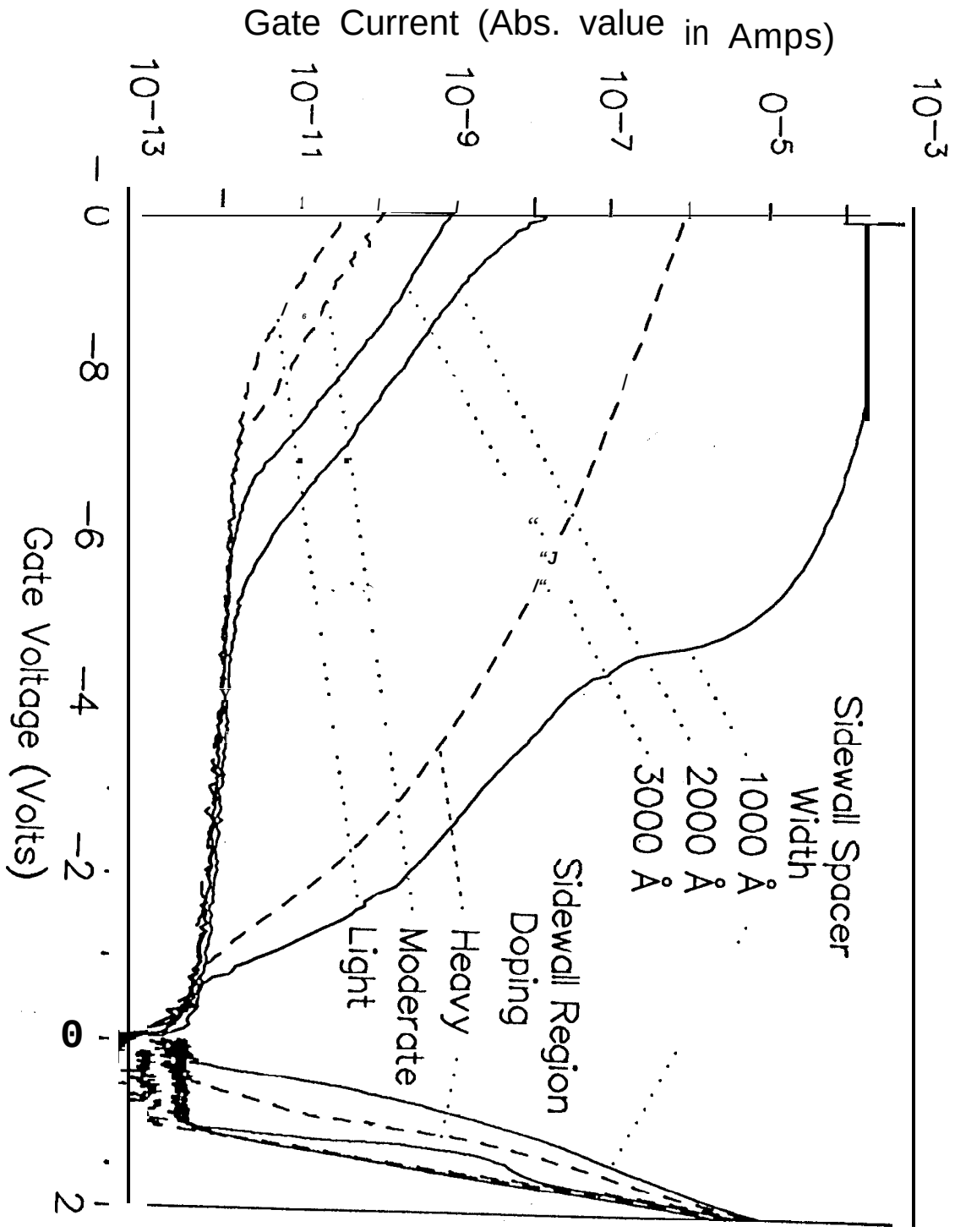

-Sidewall Spacers
source
Gate
Drain
AlGaAs Dielectric
InGaAs Channel
GaAs Buffer
GaAs Substrate

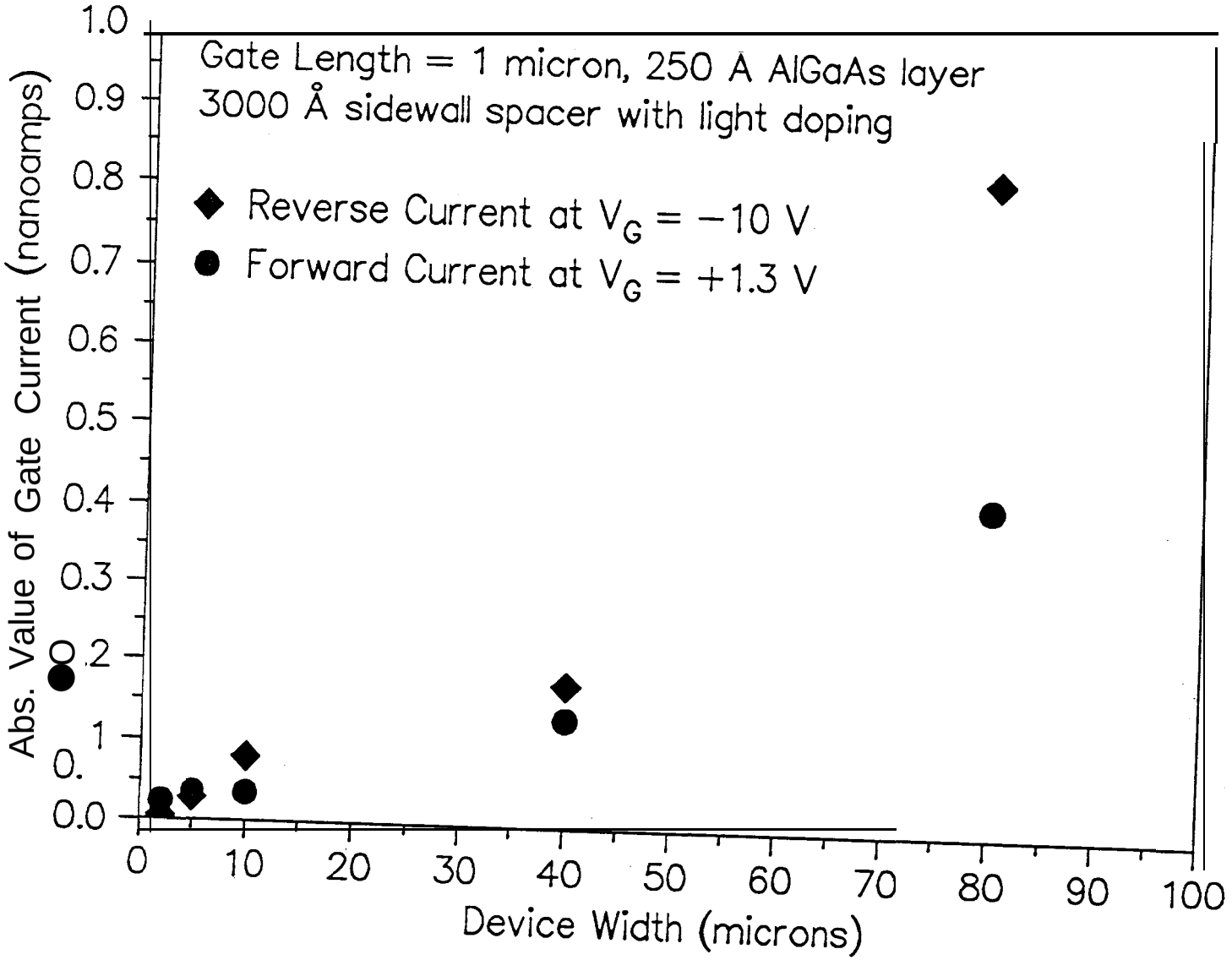

Drain Current (mA)
0.0
0.1
0.2
0.3
0.4
0.5
N-channel CHFET
10x10 μm (LxW)
4 K
V_G = 2.5 v
V_G = 2.0 v
V_G = 1.5 v
Drain Voltage (V)
0
1
2
3
4

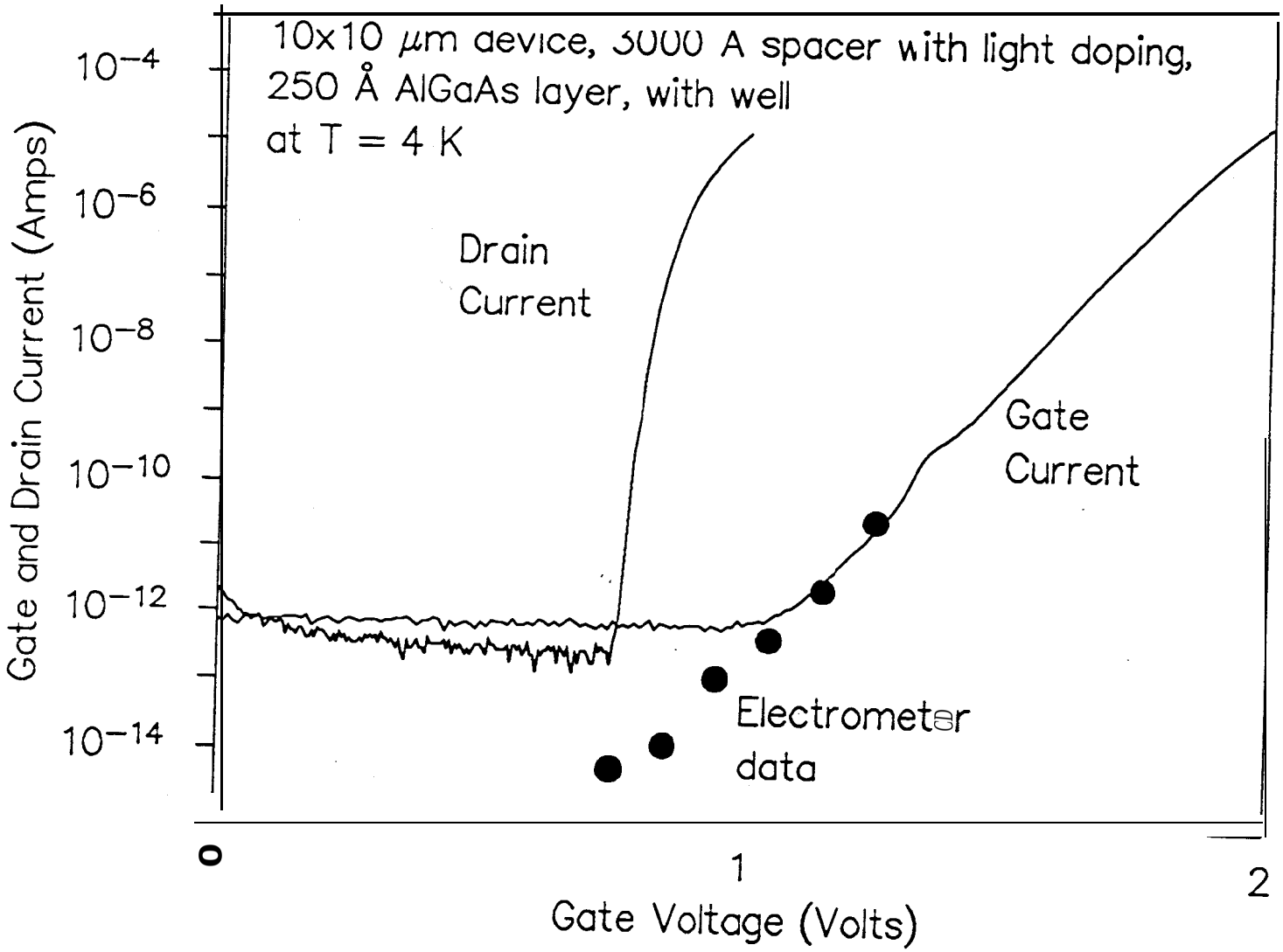

Drain Current (mA)
0.00
0.02
0.04
0.06
0.08
0.10
0.12
P-channel CHFET
10x10 μm (LxW)
4 K
V = −2.5 v
V = −2.0 v
V = −1.5 v
V = −1.0 v
Drain Voltage (V)
−4
−3
−2
−1
0

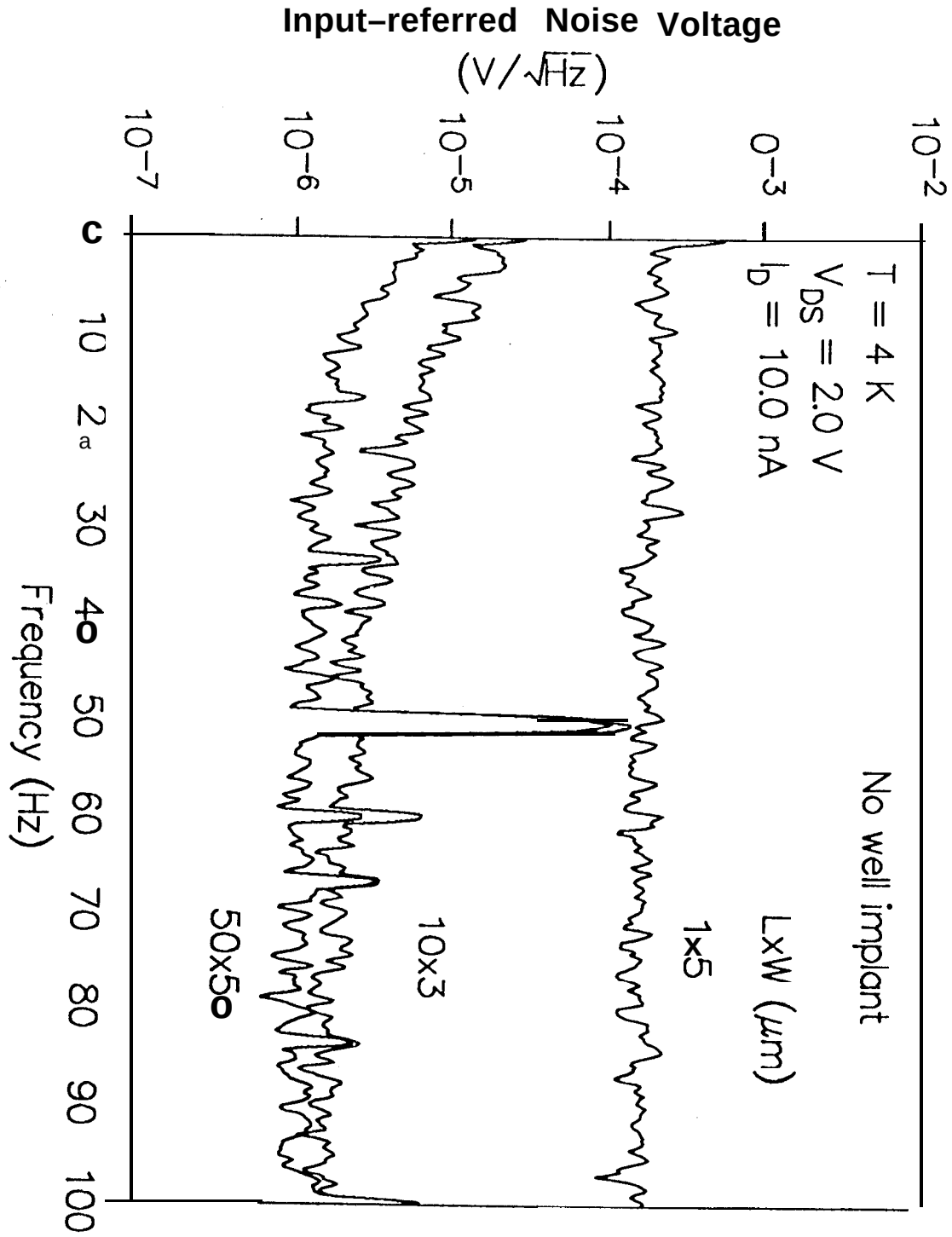

Drain current (amps)
10−3
10−4
10−5
10−6
10−7
10−8
10−9
10−10
10−11
10−12
N−channel CHFET
T = 4 K
L x W (μm)
1x80
1x40
1x10
10x10
10x3
0
1
2
Gate Voltage (Volts)

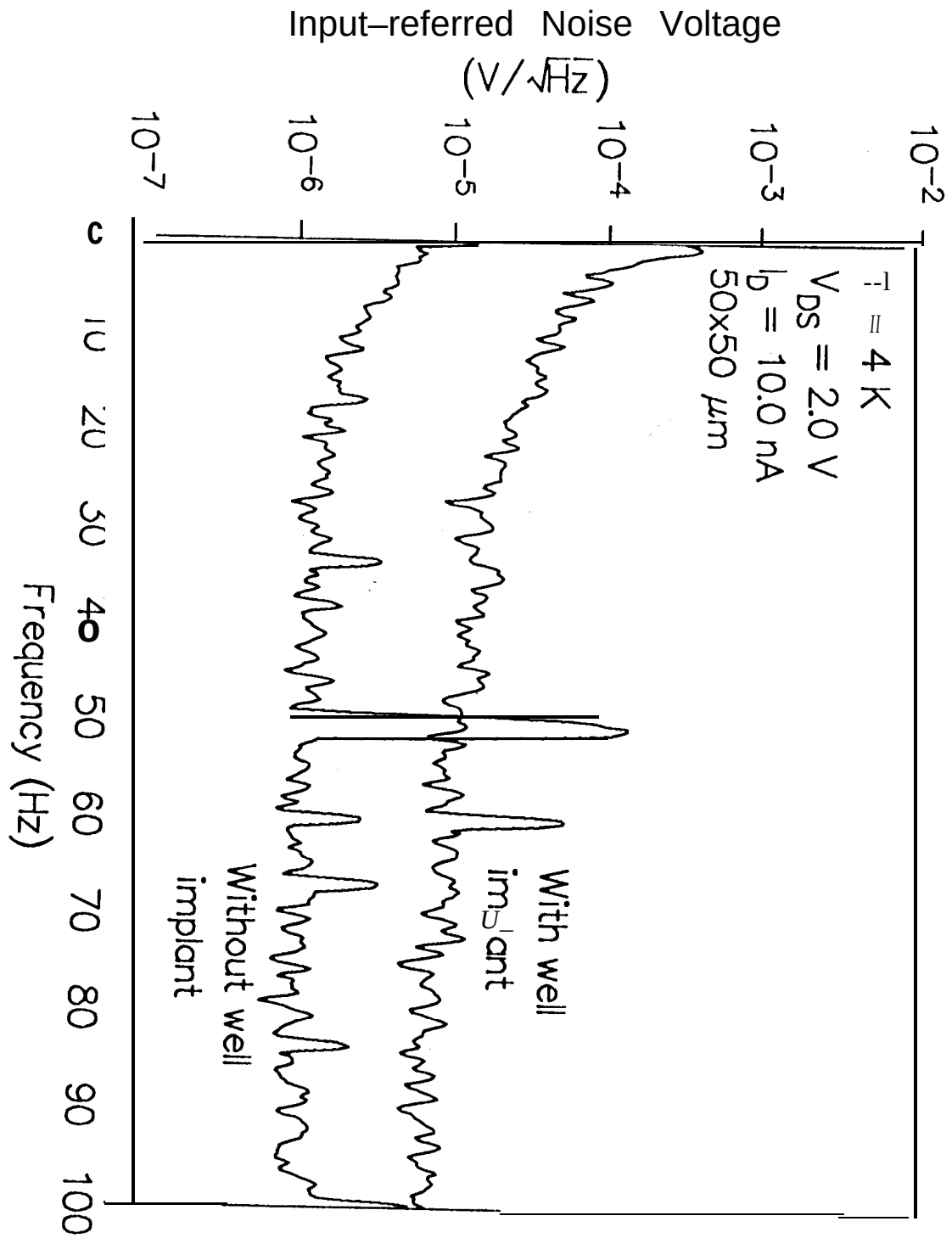

Exponent Voltage (mV)
0
10
20
30
40
0x10 μm N-channel CHFET
No well implant
V = kBT
0
100
200
300
Temperature (K)

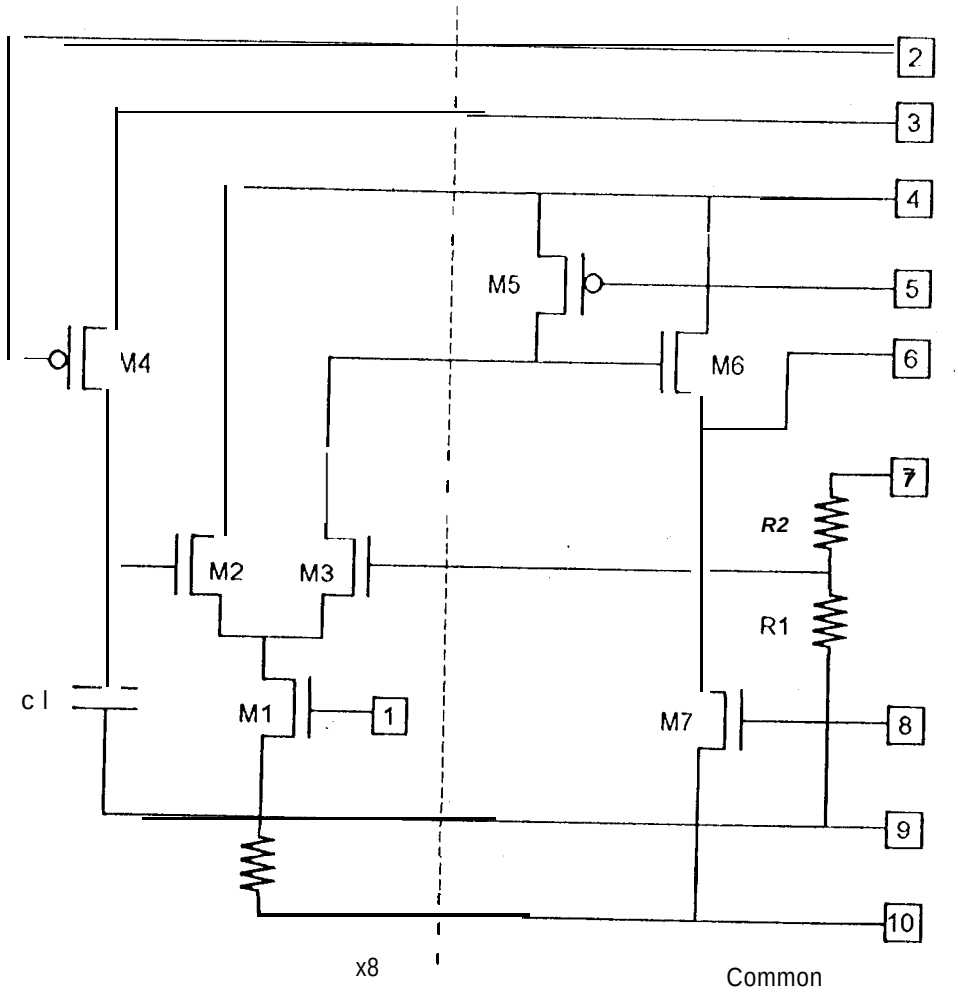

Gate Current (Abs. value in Amps)
10−3
10−5
10−7
10−9
10−11
10−13
0
−2
−4
−6
−8
Gate Voltage (Volts)
Sidewall Spacer Width
1000 Å
2000 Å
3000 Å
Sidewall Region Doping
Heavy
Moderate
Light

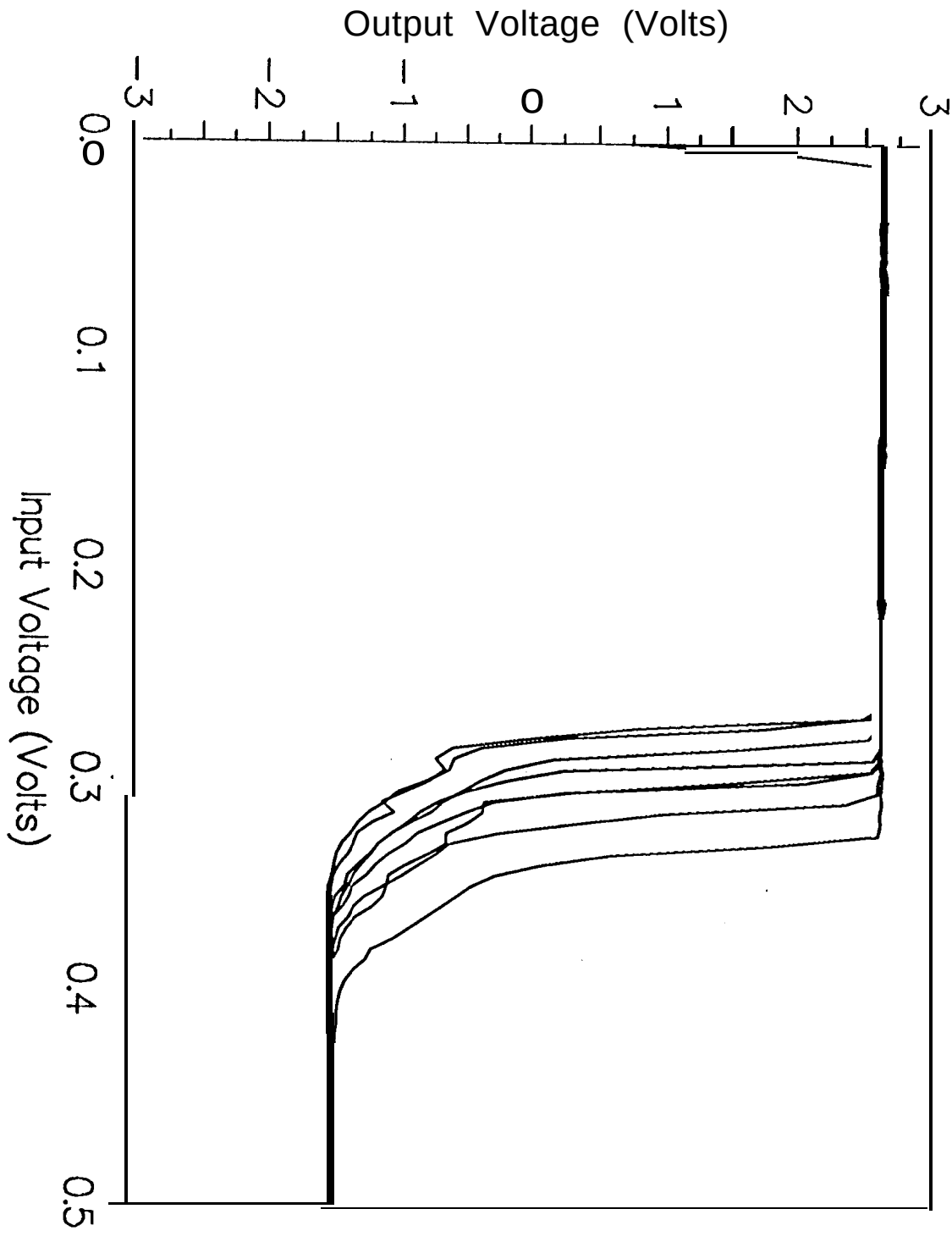

Gate Length = 1 micron, 250 Å AlGaAs layer
3000 Å sidewall spacer with light doping
Reverse Current at $V_G = -10$ V
Forward Current at $V_G = +1.3$ V
Abs. Value of Gate Current (nanoamps)
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
0
10
20
30
40
50
60
70
80
90
100
Device Width (microns)


10x10 μm device, 3000 A spacer with light doping,
250 Å AlGaAs layer, with well
at T = 4 K
Drain
Current
Gate
Current
Electrometer
data
Gate and Drain Current (Amps)
10−4
10−6
10−8
10−10
10−12
10−14
0
1
2
Gate Voltage (Volts)


Input-referred Noise Voltage
(V/√Hz)
10−2
10−3
10−4
10−5
10−6
10−7
T = 4 K
VDS = 2.0 V
ID = 10.0 nA
No well implant
LxW (μm)
1x5
10x3
50x50
c
10
2a
30
40
50
60
70
80
90
100
Frequency (Hz)


Input–referred Noise Voltage
(V/√Hz)
10−2
10−3
10−4
10−5
10−6
10−7
4 K
VDS = 2.0 V
ID = 10.0 nA
50x50 μm
With well
implant
Without well
implant
Frequency (Hz)
10
20
30
40
50
60
70
80
90
100


2
3
4
5
6
7
M5
M4
M6
R2
M2
M3
R1
c l
M1
1
M7
8
9
10
x8
Common


Output Voltage (Volts)
-3
-2
-1
0
1
2
3
0.0
0.1
0.2
0.3
0.4
0.5
Input Voltage (Volts)